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Performance of a hardware-assisted real-time garbage collector

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↑ ABSTRACT

Hardware-assisted real-time garbage collection offers high throughput and small worst-case bounds on the times required to allocate dynamic objects and to access the memory contained within previously allocated objects. Whether the proposed technology is cost effective depends on various choices between configuration alternatives. This paper reports the performance of several different configurations of the hardware-assisted real-time garbage collection system subjected to several different workloads. Reported measurements demonstrate that hardware-assisted real-time garbage collection is a viable alternative to traditional explicit memory management techniques, even for low-level languages like C++.

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Note: OCR errors may be found in this Reference List extracted from the full text article. ACM has opted to expose the complete List rather than only correct and linked references.

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↑ INDEX TERMS

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↳ **D.3.4** Processors

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1 Relational profiling: enabling thread-level parallelism in virtual machines
Timothy Heil, James E. Smith
December 2000 **Proceedings of the 33rd annual ACM/IEEE international symposium on Microarchitecture**
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2 Exploiting prolific types for memory management and optimizations
Yefim Shuf, Manish Gupta, Rajesh Bordawekar, Jaswinder Pal Singh
January 2002 **ACM SIGPLAN Notices , Proceedings of the 29th ACM SIGPLAN-SIGACT symposium on Principles of programming languages**, Volume 37 Issue 1
Full text available: pdf(203.59 KB) Additional Information: full citation, abstract, references, citings

In this paper, we introduce the notion of *prolific* and *non-prolific* types, based on the number of instantiated objects of those types. We demonstrate that distinguishing between these types enables a new class of techniques for memory management and data locality, and facilitates the deployment of known techniques. Specifically, we first present a new *type-based* approach to garbage collection that has similar attributes but lower cost than generational collection. Then we de ...

3 Concurrent garbage collection using hardware-assisted profiling
Timothy H. Heil, James E. Smith
October 2000 **ACM SIGPLAN Notices , Proceedings of the 2nd international symposium on Memory management**, Volume 36 Issue 1
Full text available: pdf(1.74 MB) Additional Information: full citation, abstract, citings, index terms

In the presence of on-chip multithreading, a Virtual Machine (VM) implementation can readily take advantage of *service threads* for enhancing performance by performing tasks such as profile collection and analysis, dynamic optimization, and garbage collection concurrently with program execution. In this context, a hardware-assisted profiling mechanism is proposed. The *Relational Profiling Architecture* (RPA) is designed from the top down. RPA is based on a relational model similar ...

4 Improving Java performance using hardware translation
Ramesh Radhakrishnan, Ravi Bhargava, Lizy K. John

June 2001 **Proceedings f the 15th internati nal c nference n Superc mputing**

Full text available: pdf(254.91 KB) Additional Information: full citation, abstract, references, citings, index terms

State of the art Java Virtual Machines with Just-In-Time (JIT) compilers make use of advanced compiler techniques, run-time profiling and adaptive compilation to improve performance. However, these techniques for alleviating performance bottlenecks are more effective in long running workloads, such as server applications. Short running Java programs, or client workloads, spend a large fraction of their execution time in compilation instead of useful execution when run using JIT compilers. In ...

5 Using complete system simulation to characterize SPECjvm98 benchmarks

Tao Li, Lizy Kurian John, Vijaykrishnan Narayanan, Anand Sivasubramaniam, Jyotsna Sabarinathan, Anupama Murthy

May 2000 **Proceedings of the 14th international conference on Supercomputing**

Full text available: pdf(1.66 MB) Additional Information: full citation, abstract, references, citings, index terms

Complete system simulation to understand the influence of architecture and operating systems on application execution has been identified to be crucial for systems design. While there have been previous attempts at understanding the architectural impact of Java programs, there has been no prior work investigating the operating system (kernel) activity during their executions. This problem is particularly interesting in the context of Java since it is not only the application that can invoke ...

6 Exploiting ILP in page-based intelligent memory

Mark Oskin, Justin Hensley, Diana Keen, Frederic T. Chong, Matthew Farrens, Aneet Chopra

November 1999 **Proceedings of the 32nd annual ACM/IEEE international symposium on Microarchitecture**

Full text available: pdf(1.35 MB) Publisher Site Additional Information: full citation, abstract, references, index terms

This study compares the speed, area, and power of different implementations of Active Pages [OCS98], an intelligent memory system which helps bridge the growing gap between processor and memory performance by associating simple functions with each page of data. Previous investigations have shown up to 1000X speedups using a block of reconfigurable logic to implement these functions next to each sub-array on a DRAM chip. In this study, we show that instruction-level parallelism, n ...

7 Garbage collection for strongly-typed languages using run-time type reconstruction

Shail Aditya, Christine H. Flood, James E. Hicks

July 1994 **ACM SIGPLAN Lisp Pointers , Proceedings of the 1994 ACM conference on LISP and functional programming**, Volume VII Issue 3

Full text available: pdf(1.40 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Garbage collectors perform two functions: live-object detection and dead-object reclamation. In this paper, we present a new technique for live-object detection based on run-time type reconstruction for a strongly typed, polymorphic language. This scheme uses compile-time type information together with the run-time tree of activation frames to determine the exact type of every object participating in the computation. These reconstructed types are then used ...

8 Fast out-of-order processor simulation using memoization

Eric Schnarr, James R. Larus

October 1998 **Pr ceedings f the eighth international c nference n Architectural supp rt f r pr gramming languages and perating systems**, Volume 32 , 33

Issue 5 , 11

Full text available: pdf(1.43 MB) Additional Information: full citation, abstract, references, citings, index terms

Our new out-of-order processor simulatol; FastSim, uses two innovations to speed up simulation 8--15 times (vs. Wisconsin SimpleScalar) with no loss in simulation accuracy. First, FastSim uses speculative direct-execution to accelerate the functional emulation of speculatively executed program code. Second, it uses a variation on memoization---a well-known technique in programming language implementation---to cache microarchitecture states and the resulting simulator actions, and then "fast forw ...

Keywords: direct-execution, memoization, out-of-order processor simulation

9 The cache behaviour of large lazy functional programs on stock hardware

Nicholas Nethercote, Alan Mycroft

June 2002 **ACM SIGPLAN Notices , Proceedings of the workshop on Memory system performance**, Volume 38 Issue 2 supplement

Full text available: pdf(1.26 MB) Additional Information: full citation, abstract, references, index terms

Lazy functional programs behave differently from imperative programs and these differences extend to cache behaviour. We use hardware counters and a simple yet accurate execution cost model to analyse some large Haskell programs on the x86 architecture. The programs do not interact well with modern processors---L2 cache data miss stalls and branch misprediction stalls account for up to 60% and 32% of execution time respectively. Moreover, the program code exhibits little exploitable instruction- ...

Keywords: Glasgow Haskell Compiler, Haskell, branch misprediction, cache measurement, cache simulation, hardware counters

10 A survey of processors with explicit multithreading

Theo Ungerer, Borut Robič, Jurij Šilc

March 2003 **ACM Computing Surveys (CSUR)**, Volume 35 Issue 1

Full text available: pdf(920.16 KB) Additional Information: full citation, abstract, references, index terms

Hardware multithreading is becoming a generally applied technique in the next generation of microprocessors. Several multithreaded processors are announced by industry or already into production in the areas of high-performance microprocessors, media, and network processors.A multithreaded processor is able to pursue two or more threads of control in parallel within the processor pipeline. The contexts of two or more threads of control are often stored in separate on-chip register sets. Unused i ...

Keywords: Blocked multithreading, interleaved multithreading, simultaneous multithreading

11 Performance of a hardware-assisted real-time garbage collector

William J. Schmidt, Kelvin D. Nilsen

November 1994 **Proceedings of the sixth international conference on Architectural support for programming languages and operating systems**, Volume 29 , 28 Issue 11 , 5

Full text available: pdf(1.16 MB) Additional Information: full citation, abstract, references, citings, index terms

Hardware-assisted real-time garbage collection offers high throughput and small worst-case bounds on the times required to allocate dynamic objects and to access the memory contained within previously allocated objects. Whether the proposed technology is cost

effective depends on various choices between configuration alternatives. This paper reports the performance of several different configurations of the hardware-assisted real-time garbage collection system subjected to several different ...

12 MEDEA workshop: Fresh Breeze: a multiprocessor chip architecture guided by modular programming principles

Jack B. Dennis

March 2003 **ACM SIGARCH Computer Architecture News**, Volume 31 Issue 1

Full text available: pdf(862.10 KB) Additional Information: full citation, abstract, references, index terms

It is well-known that multiprocessor systems are vastly more difficult to program than systems that support sequential programming models. In a 1998 paper[11] this author argued that six important principles for supporting modular software construction are often violated by the architectures proposed for multiprocessor computer systems. The Fresh Breeze project concerns the architecture and design of a multiprocessor chip that can achieve superior performance while honoring these six principles. ...

13 Stride prefetching by dynamically inspecting objects

Tatsushi Inagaki, Tamiya Onodera, Hideaki Komatsu, Toshio Nakatani

May 2003 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 2003 conference on Programming language design and implementation**, Volume 38 Issue 5

Full text available: pdf(168.64 KB) Additional Information: full citation, abstract, references, citings, index terms

Software prefetching is a promising technique to hide cache miss latencies, but it remains challenging to effectively prefetch pointer-based data structures because obtaining the memory address to be prefetched requires pointer dereferences. The recently proposed stride prefetching overcomes this problem, but it only exploits *inter-iteration* stride patterns and relies on an off-line profiling method.We propose a new algorithm for stride prefetching which is intended for use in a dynamic ...

Keywords: Java just-in-time compiler, object inspection, stride prefetching

14 Cycles to recycle: garbage collection to the IA-64

Richard L. Hudson, J. Elliot Moss, Sreenivas Subramoney, Weldon Washburn

October 2000 **ACM SIGPLAN Notices , Proceedings of the 2nd international symposium on Memory management**, Volume 36 Issue 1

Full text available: pdf(1.25 MB) Additional Information: full citation, abstract, citings, index terms

The IA-64, Intel's 64-bit instruction set architecture, exhibits a number of interesting architectural features. Here we consider those features as they relate to supporting garbage collection (GC). We aim to assist GC and compiler implementors by describing how one may exploit features of the IA-64. Along the way, we record some previously unpublished object scanning techniques, and offer novel ones for object allocation (suggesting some simple operating system support that would simplify it ...

15 Memory forwarding: enabling aggressive layout optimizations by guaranteeing the safety of data relocation

Chi-Keung Luk, Todd C. Mowry

May 1999 **ACM SIGARCH Computer Architecture News , Proceedings of the 26th annual internati nal symp sium n C mputer architecture**, Volume 27 Issue 2

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By optimizing data layout at run-time, we can potentially enhance the performance of

caches by actively creating spatial locality, facilitating prefetching, and avoiding cache conflicts and false sharing. Unfortunately, it is extremely difficult to guarantee that such optimizations are *safe* in practice on today's machines, since accurately updating *all* pointers to an object requires perfect alias information, which is well beyond the scope of the compiler for languages such as C. T ...

16 Sentinel scheduling for VLIW and superscalar processors

Scott A. Mahlke, William Y. Chen, Wen-mei W. Hwu, B. Ramakrishna Rau, Michael S. Schlansker

September 1992 **ACM SIGPLAN Notices , Proceedings of the fifth international conference on Architectural support for programming languages and operating systems**, Volume 27 Issue 9

Full text available: pdf(1.22 MB) Additional Information: full citation, abstract, references, citings, index terms

Speculative execution is an important source of parallelism for VLIW and superscalar processors. A serious challenge with compiler-controlled speculative execution is to accurately detect and report all program execution errors at the time of occurrence. In this paper, a set of architectural features and compile-time scheduling support referred to as sentinel scheduling is introduced. Sentinel scheduling provides an effective framework for compiler-controlled speculative ex ...

17 Performance: Method-level phase behavior in java workloads

Andy Georges, Dries Buytaert, Lieven Eeckhout, Koen De Bosschere

October 2004 **Proceedings of the 19th annual ACM SIGPLAN Conference on Object-oriented programming, systems, languages, and applications**

Full text available: pdf(695.63 KB) Additional Information: full citation, abstract, references, index terms

Java workloads are becoming more and more prominent on various computing devices. Understanding the behavior of a Java workload which includes the interaction between the application and the virtual machine (VM), is thus of primary importance during performance analysis and optimization. Moreover, as contemporary software projects are increasing in complexity, automatic performance analysis techniques are indispensable. This paper proposes an off-line method-level phase analysis approach for ...

18 Superscalar design: Three extensions to register integration

Vlad Petric, Anne Bracy, Amir Roth

November 2002 **Proceedings of the 35th annual ACM/IEEE international symposium on Microarchitecture**

Full text available: pdf(1.37 MB) Additional Information: full citation, abstract, references, index terms
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Register integration (or just integration) is a register renaming discipline that implements instruction reuse via physical register sharing. Initially developed to perform squash reuse, the integration mechanism can exploit more reuse scenarios. Here, we describe three extensions to the original design that expand its applicability and boost its performance impact. First, we extend squash reuse to general reuse. Whereas squash reuse maintains the concept of an instruction instance "owning" its ...

19 The use of multithreading for exception handling

Craig B. Zilles, Joel S. Emer, Gurindar S. Sohi

November 1999 **Pr ceedings f the 32nd annual ACM/IEEE internati nal symp sium n Micr architecture**

Full text available: pdf(1.49 MB) Additional Information: full citation, abstract, references, citings, index terms
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Common hardware exceptions, when implemented by trapping, unnecessarily serialize program execution in dynamically scheduled superscalar processors. To avoid the consequences of trapping the main program thread, multithreaded CPUs can exploit control and data independence by executing the exception handler in a separate hardware context. The main thread doesn't squash instructions after the excepting instruction, conserving fetch bandwidth and allowing execution of instructions inde ...

20 EPIC compilation: Optimization for the Intel® Itanium® architecture register stack

Alex Settle, Daniel A. Connors, Gerolf Hoflehner, Dan Lavery

March 2003 **Proceedings of the international symposium on Code generation and optimization: feedback-directed and runtime optimization**

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The Intel® Itanium® architecture contains a number of innovative compiler-controllable features designed to exploit instruction level parallelism. New code generation and optimization techniques are critical to the application of these features to improve processor performance. For instance, the Itanium® architecture provides a compiler-controllable virtual register stack to reduce the penalty of memory accesses associated with procedure calls. The Itanium® Register Stack Engine ...

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Jae-Woo Ahn; Soo-Mook Moon; Wonyong Sung;
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2 **Design study of shared memory in VLIW video signal processors**
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3 **Reducing cost and tolerating defects in page-based intelligent mem**
Oskin, M.; Keen, D.; Hensley, J.; Lita, L.-V.; Chong, F.T.;
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4 **A semi-f lded instructi n f rmat f r VLIW architecture**
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[Abstract] [PDF Full-Text (388 KB)] IEEE CNF

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5 **Expl iting ILP in page-based intelligent mem ry**
Oskin, M.; Hensley, J.; Keen, D.; Chong, F.T.; Farrens, M.; Chopra, A.;
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6 **A microprocessor with a 128-bit CPU, ten floating-point MAC's, four floating-point dividers, and an MPEG-2 decoder**
Suzuoki, M.; Kutaragi, K.; Hiroi, T.; Magoshi, H.; Okamoto, S.; Oka, M.; Ohba Yamamoto, Y.; Furuhashi, M.; Tanaka, M.; Yutaka, T.; Okada, T.; Nagamatsu, Urakawa, Y.; Funyu, M.; Kunimatsu, A.; Goto, H.; Hashimoto, K.; Ide, N.; Murakami, H.; Ohtaguro, Y.; Aono, A.;
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7 **Modulo scheduling for a fully-distributed clustered VLIW architectur**
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12 **Multi-thread VLIW processor architecture for HDTV decoding**
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21 **GFLOPS: a general flexible linearly organized parallel structure f r images**
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